REMARKS

Claims 1-16 and 21-23 are pending in the present application. All of these claims stand rejected. Applicant respectfully traverses and requests reconsideration of the rejections based on the following remarks.

Claims 1-2, 5-9, and 21-22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Urakawa (U.S. Published Application No. 2003/0015792). The Applicants respectfully traverse this rejection for the following reasons.

Concerning independent claim 1, the Office Action asserts that Urakawa teaches all of the claimed elements. The Applicants respectfully disagree for the following reasons.

First, claim 1 features "a standard dimension substrate." Urakawa fails to teach this claimed element. Rather, page 6 of Urakawa merely refers to conventional memory chips having particular sizes, but fails to teach or suggest that the substrate on which these devices are mounted has a standard dimension as featured in claim 1.

Claim 1 also features "an information router integrated on the carrier substrate." The Office Action equates that the logic chip illustrated in Figs. 19-21 is equivalent to this claimed feature. Urakawa, however, merely discloses that the "logic chip" is an LSI chip (see paragraph 0048, for example) and does not specifically contemplate that the disclosed System On a Chip (SOC) includes an actual information router, such as a Northbridge (See, e.g., Fig. 2 of the present application).

Finally, claim 1 features a "system memory operative to store system instructions also integrated on the carrier substrate ... when the system instructions may be stored and retrieved from the system memory through the information router." Urakawa does not teach or suggest that the memory chips disclosed therein include a system memory "wherein system instructions may be stored and retrieved from this memory through [an] information router." Rather, the examples of Urakawa teach a complete system on a chip (SOC) having a logic circuit connected to a memory directly. Accordingly, there would be no information router needed in Urakawa and the corresponding need to route system instructions to be stored and retrieved from the

system memory. As an example, the present application discloses an integrated circuit, such as circuit 204 illustrated in Fig. 2, where the system memory 208 for the entire system 200 stores and receives system instructions, such as system instructions from a CPU 202 via a data router 206. This is simply not taught by Urakawa as system is contained in a single SOC device and thus no information routing via an information router (e.g., a Northbridge) is brought on when needed.

Accordingly, in light of the above comments, Applicants respectfully submit that Urakawa does not anticipate the subject matter of claim 1.

With respect to dependent claims 2 and 5-9, these claims are submitted to allowable on their merits and also due to their dependency on independent claim 1.

With respect to claims 21 and 22, these claims are also submitted to be allowable at least for the same reasons presented above with respect to claim 1.

Claims 3-4, 10-16, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Urakawa in view of Melo et al. (U.S. Patent No. 6,243,817). The Applicants respectfully traverse this rejection for the following reasons.

In rejecting the above-enumerated claims, the Office Action asserts that Urakawa discloses all of the claimed elements except inclusion of graphics chips or a Northbridge. First, as argued previously, the Applicants respectfully disagree and submit that Urakawa does not disclose the elements for which it is alleged to contain.

Moreover, with respect to claims 3 and 4, these claims are submitted to be allowable on their merits and also due to their dependency on independent claim 1.

With respect to independent claim 10, the Office Action appears to allege that Melo discloses a common substrate including the graphics accelerator 20 and the Northbridge 14. It is not clear to Applicants, however, where this specific teaching is contained within Melo and the Office Action does not specifically point to any sections in the reference concerning this teaching. Nonetheless, Melo does not teach or suggest the features of claims including a

standard dimension carrier substrate with an application specific integrated circuit die having a Northbridge coupled to the carrier substrate as well as a system memory operative to store system instructions also integrated on the carrier substrate where the system instructions are stored and retrieved through the Northbridge within the packaged chip. No teaching or suggestion appears in Melo to this effect. As argued previously, Urakawa also fails to teach or suggest these features. Accordingly, Applicants respectfully submit that the cited references, either combined or taken separately, fail to teach or suggest all of the elements of claim 10.

With respect to dependent claims 11-16 and 23, Applicants respectfully submit that these claims are allowable on their merits and also based on their respective dependencies.

In light of the forgoing comments, Applicants respectfully submit that the application is in condition for allowance and request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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